In the specification:

Please amend the paragraph beginning on page 7, line 6 and ending on page 8, line 5 as follows:

A more complete understanding of the system and method of the present invention may be obtained by reference to the following Detailed Description when taken in conjunction with the accompanying Drawings wherein:

Figures 1A and 1B are circuit schematics of conventional 1T1C and 2T2C ferroelectric memory cells, respectively;

Figure 2 illustrates a conventional timing diagram for the read and restore operation of a ferroelectric memory cell;

Figure 3 illustrates the polarization characteristics of a ferroelectric memory cell operating under normal conditions and degraded conditions;

Figure 4 is a block diagram of a memory device according to an embodiment of the present invention;

Figure 5 is a test circuit for the memory device of Figure 4;

Figure 6 is an alternative embodiment of a portion of the test circuit for the memory device of Figure 4;

Figure 7 is a calibration test circuit for the test circuit of Figure 5;

Figure 8 is a flow chart illustrating an operation of the calibration test circuit of Figure 7; [and]

Figure 9 is a flow chart illustrating a test operation of the memory device of Figure 4; and

Figure 10 is a block diagram of an apparatus incorporating the memory device of Figure 4.

After the paragraph beginning on page 20, line 1 and ending on page 20, line 10, please add the following new paragraph:

--Referring to Figure 10, memory device 1 may form part of an apparatus including a processing unit having an address port connected to an address input port of memory device 1 and a data port connected to a data port of memory device 1.--.

In the claims:

Please cancel claims 38 and 39 without prejudice and without abandonment of the subject matter thereof.

Please amend the claims as follows:

16. (Amended) A method of testing a semiconductor memory device having an array of memory cells and sense amplifier circuitry coupled to bit lines of the array, the semiconductor memory device being in (an integrated circuit chip), the method comprising:

connecting memory cells in a row of memory cells to bit lines of the array;